WHAT IS CLAIMED IS:

1. A circuit for domino logic wherein an output of the domino logic is based upon a charge on a domino node in response to multiple logic signals, the circuit comprising:
a first keeper transistor having a gate coupled with the output;
a second keeper transistor having a channel coupled in series with a channel of the first keeper transistor, the channels being between a high voltage source and the domino node; and
an input transistor having a gate coupled with a logic signal of the multiple logic signals and a channel coupled between a gate of the second keeper transistor and the high voltage source.

2. The circuit of claim 1, further comprising an accelerator transistor having a gate coupled with the gate of the second keeper transistor and a channel coupled between a low voltage source and the domino node.

3. The circuit of claim 1, further comprising a clock transistor having a gate coupled with a clock input, and a channel coupled between the high voltage and the channel of the input transistor.

4. The circuit of claim 1, further comprising a pre-charge transistor having a gate coupled with the domino node and a channel coupled between the gate of the second keeper transistor and a low voltage source.

5. The circuit of claim 1, wherein the input transistor couples with the high voltage source via a channel of at least one other input transistor, the at least one other input transistor having a gate coupled with another logic signal of the multiple logic signals.

6. The circuit of claim 1, wherein the input transistor couples with the high voltage source in parallel with a channel of at least one other input transistor, the at least one other input transistor having a gate coupled with another logic signal of the multiple logic signals.

7. The circuit of claim 1, wherein the input transistor receives the logic signal substantially simultaneously with receipt of the logic signal by another input transistor having a channel coupled between the domino node and a low voltage source.

8. An apparatus comprising:

a logic input circuit to draw current from a domino node to generate a first logical output during a portion of a clock cycle;

a clock circuit to couple the logic input circuit with a low voltage source during the portion of the clock cycle;

an output circuit coupled to the domino node to output a second logical output when the domino node is above a threshold voltage; and

a keeper circuit to pull up the domino node in response to the output when the domino node is at a high voltage and to stop pulling up the domino node before the output circuit outputs the first logical output.

9. The apparatus of claim 8, wherein the logic input circuit comprises an input transistor to turn on to trigger the first logical output in response to a logic signal input, pulling down the domino node via a channel of the input transistor.

10. The apparatus of claim 9, wherein a channel of the input transistor is coupled in series with a channel of a second transistor that responds to a second logic signal, the channel of the second transistor being between the clock circuit and the channel of the input transistor.

11. The apparatus of claim 9, wherein a channel of the input transistor is coupled in parallel with a channel of a second transistor that responds to a second logic signal, the channel of the second transistor being coupled between the clock circuit and the domino node.

12. The apparatus of claim 8, wherein keeper circuit comprises a keeper transistor having a gate coupled with the output circuit, and a channel coupled between the high voltage source and the domino node via a third transistor, wherein the third transistor comprises a gate coupled to a mirror input circuit, the mirror input circuit to couple the gate of the third transistor to the high voltage source to turn off the third transistor when the logic input circuit draws current from the domino node.

13. The apparatus of claim 12, further comprising an accelerator circuit having an input coupled with the mirror input circuit to couple the domino node to the low voltage source when the logic input circuit draws current from the domino node.

14. The apparatus of claim 12, wherein the mirror input circuit comprises transistors having small junction capacitances.

15. The apparatus of claim 8, wherein the logic input circuit comprises transistors having small junction capacitances.

16. A method for enhancing domino logic, the method comprising:
removing charge from a domino node via a first path in response to a logic signal;
supplying charge from a high voltage source to a second node in response to the logic signal, the charge on the second node opening a second path to remove charge from the domino node; and
generating an output based upon the removal of charge from the domino node.

17. The method of claim 16, wherein removing charge comprises turning on a low threshold transistor with the logic signal to couple the domino node with a low voltage source.

18. The method of claim 16, wherein supplying charge comprises turning on a low threshold transistor with the logic signal to couple the second node with the high voltage source.

19. The method of claim 16, wherein supplying charge comprises increasing the voltage of the second node to a threshold voltage of an accelerator transistor to turn on the accelerator transistor, creating the second path via the channel of the accelerator transistor to a low voltage source.

20. The method of claim 19, wherein increasing the voltage comprises increasing the voltage to a threshold voltage of a pull-up transistor to block a third path between the high voltage source and the domino node.